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Attorneys for Plaintiffs and Counterdefendants
 ALPHA & OMEGA SEMICONDUCTOR,
 LTD.
 ALPHA & OMEGA SEMICONDUCTOR,
 INC.

UNITED STATES DISTRICT COURT
 NORTHERN DISTRICT OF CALIFORNIA
 SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR,
 LTD., a Bermuda corporation; and
 ALPHA & OMEGA SEMICONDUCTOR,
 INC., a California corporation,

Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR
 CORP., a Delaware corporation,

Defendant and Counterclaimant.

AND RELATED COUNTERCLAIMS.

Case No. C 07-2638 JSW
 (Consolidated with Case No. C-07-2664 JSW)

**DECLARATION OF C. ANDRE T.
 SALAMA, PH.D. IN SUPPORT OF ALPHA
 & OMEGA SEMICONDUCTOR, LTD AND
 ALPHA & OMEGA SEMICONDUCTOR,
 INC'S OPENING CLAIM
 CONSTRUCTION BRIEF PURSUANT TO
 CIVIL L. R. 16-11(D)(1)**

Date: June 4, 2008
 Time: 2:00 PM
 Place: Courtroom 2, 17th Floor
 Judge: Honorable Jeffrey S. White

1 I, C. Andre T. Salama, hereby declare as follows:

2 1. I am a University Professor (Emeritus) at the University of Toronto in the
3 Department of Electrical and Computer Engineering, 10 King's College Road, Toronto, Ontario,
4 M5S 3G4, Canada. I have been retained as a consultant for the Plaintiffs and counterdefendants
5 Alpha & Omega Semiconductor, LTD and Alpha & Omega Semiconductor, Inc., in the present
6 action. I submit this declaration in support of Alpha & Omega Semiconductor, LTD and Alpha &
7 Omega Semiconductor, Inc.'s Opening Claim Construction Brief Pursuant to Civil L. R. 16-
8 11(d)(1).

9 2. The small wire at the bottom right of Fig. 2C of the '567 Patent connects the gate
10 contact area of the device to the lead frame. The gate contact area of the device is the small
11 square where the small wire is attached. The remaining eleven longer wires are connected to the
12 source contact area of the device.

13 3. The phrase "applying a polysilicon mask for etching said polysilicon layer to
14 define a plurality of polysilicon gates" is unambiguous. Etching is a well-known process, and a
15 mask is usually applied to the surface of the substrate before etching in order to select what areas
16 will be etched away. Gates are a component of all MOSFETs, and the gates are generally defined
17 by etching. Etching defines the dimensions of the gates. Also, polysilicon is widely used as a
18 gate material.

19 4. Fabrication of a power MOSFET typically includes multiple etching operations,
20 and typically a mask is applied before each etching operation. Both the process of etching and
21 the process of applying a mask are well-known. Different materials and chemicals are used for
22 masking and etching depending on the layer to be etched.

23 5. Before etching, a mask is typically applied to cover part of the device surface. By
24 covering some areas of the device surface and not other areas, the mask defines what areas will be
25 etched. Etching removes material from areas of the surface that are not covered by the mask.
26 Wet chemical etching is commonly used in the fabrication of power MOSFETs, and there are
27 other etching techniques. The process of etching is well-known and has been commonly used for
28 decades.

6. One of the essential elements of a power MOSFET is the gate. The gate controls whether the power MOSFET is on or off based on the voltage applied to it. If the voltage applied to the gate exceeds the threshold voltage V_{TH} , the power MOSFET is on.

7. In a MOSFET with planar gates, a layer of gate material is formed on the surface of the substrate. The formation of this layer establishes the thickness of the gates. Etching removes material to establish the horizontal dimensions of the gate. In a MOSFET with trenched gates, trenches are first created. The trenches are lined with an insulator, then filled with gate material. The gate material is typically polysilicon. Etching is then used to remove some of the gate material from the top of the trench to establish the vertical extension of the gate into the trench.

8. An n-type semiconductor region is compensated when p-type dopants are introduced into the region. Similarly, a p-type semiconductor is compensated when n-type dopants are introduced into the region. When a semiconductor region is compensated, the introduced dopants partially cancel the pre-existing dopants of the opposite conductivity type.

9. Ion implantation involves bombarding a target with energized ions. The greater the energy of the ions, the greater the penetration of the ions into the target.

10. Practicing the teaching of the '567 patent does not require three or more of any element. In particular, a device with two gate runners, two sub-contact areas, or two lead wires in a sub-contact area operates according to the invention. The number of each of these elements is irrelevant to the operation of the device.

I declare under of penalty of perjury that the foregoing is true and correct.

Dated: March 13, 2008

by 
C. Andre T. Salama, Ph.D.